**来源：PLDA XpressSWITCH Switch IP for PCIe 4.0 User Guide: ASIC，Version 2.5.6**

**4.7 Power Management**

**4.7 电源管理**

The XpressSWITCH uses PL\_WAKE\_OEN and PL\_WAKE\_IN as legacy and native power management signals. See Section 6.2.8 for a description of these signals.

XpressSWITCH 使用 PL\_WAKE\_OEN 和 PL\_WAKE\_IN 作为传统和本机电源管理信号。有关这些信号的说明，请参见第 6.2.8 节。

**4.7.1 L2 Low-Power State**

**4.7.1 L2 低功耗状态**

PME\_TURN\_OFF and PME\_TO\_ACK messages are handled by the Core signals TLX\_PM\_L2\_CONTROL/TLX\_PM\_L2\_STATUS:

1. When the switch upstream receives the **PME\_TURN\_OFF** message on the PCIe link, its **TLX\_PM\_L2\_STATUS** output is asserted.

2. This activates the **TLX\_PM\_L2\_CONTROL** input of the downstream ports, causing a **PME\_TURN\_OFF** message to be sent downstream.

3. When the downstream ports receive the **PME\_TO\_ACK** message, their corresponding **TLX\_PM\_L2\_STATUS** output is asserted.

4. When **TLX\_PM\_L2\_STATUS** signal is set for each downstream port, the switching logic will set the **TLX\_PM\_L2\_CONTROL** signal of the upstream to notify that it is ready for L2 state entry.

PME\_TURN\_OFF 和 PME\_TO\_ACK 消息由核心信号 TLX\_PM\_L2\_CONTROL/TLX\_PM\_L2\_STATUS 处理：

1. 当交换机上游在 PCIe 链路上接收到 PME\_TURN\_OFF 消息时，其 TLX\_PM\_L2\_STATUS 输出被置位。

2. 这会激活下游端口的 TLX\_PM\_L2\_CONTROL 输入，导致向下游发送 PME\_TURN\_OFF 消息。

3. 当下游端口收到 PME\_TO\_ACK 消息时，其相应的 TLX\_PM\_L2\_STATUS 输出被置位。

4. 当为每个下游端口设置 TLX\_PM\_L2\_STATUS 信号时，切换逻辑将设置上游端口的 TLX\_PM\_L2\_CONTROL 信号，以通知其已准备好进入 L2 状态。

Note: The XpressSWITCH can enter L2 states when one or more of its ports is in a non-active state (for example, if a port is hot-plug capable but no devices are connected to the port), unless the application forces the port into an LTSSM Disabled state. In this case, the upstream port cannot enter the L2 state.

注意：当 XpressSWITCH 的一个或多个端口处于非活动状态时（例如，如果端口支持热插拔，但没有设备连接到该端口），XpressSWITCH 可以进入 L2 状态，则除非应用程序强制该端口进入 LTSSM 禁用状态。此时上游端口无法进入L2状态。

此时：当 XpressSWITCH 的一个或多个端口处于非活动状态时？还是应用程序强制该端口进入 LTSSM 禁用状态时？

**4.7.2 ASPM L0s/L1 and L1 Low-Power States**

**4.7.2 ASPM L0s/L1 和 L1 低功耗状态**

The PCI Express specifications require that switch ports add a minimal latency for low power states entry and exit processes.

PCI Express 规范要求交换机端口为低功耗状态进入和退出过程添加最小的延迟。

The XpressRICH Core implements the rule:

• A switch port should not enter Tx L0s state if its receive lanes are not in L0s.

XpressRICH Core 实施以下规则：

• 如果交换机端口的接收通道不处于 L0 状态，则交换机端口不应进入 Tx L0 状态。

The following specifications are implemented using the signal **TLN\_BRSW\_OUT/IN** bits 1 and 2 (see **Table 38**):

以下规范是使用信号 TLN\_BRSW\_OUT/IN bit 1 和 bit 2 实现的（请参阅表 38）：

• A switch upstream port should exit L0s if one of the downstream ports has exited L0s.

• 如果下游端口之一已退出 L0，则交换机上游端口应退出 L0。

• All downstream ports of a switch should exit L0s if the upstream port has exited L0s.

• 如果上游端口已退出L0s，则交换机的所有下游端口都应退出L0s。

• A switch upstream port should not initiate an L1 / ASPM L1 entry process if not all of the active downstream ports are in L1 / ASPM L1.

• 如果并非所有活动下游端口都位于 L1/ASPM L1 中，则交换机上游端口不应启动 L1/ASPM L1 进入过程。

Initiate:开始、发起

• When the XpressSWITCH receives an L1 exit request from a downstream component (Endpoint or another Switch), its upstream port exits ASPM L1 when one of its downstream ports has exited ASPM L1 to recovery. The upstream port then signals L1 exit to the Root Complex. The Root Complex responds by signaling L1 exit to the Switch upstream port. When the switch upstream port exits L1, all the downstream ports in **ASPM** L1 also exit L1 to minimize the overall exit latency of returning to L0. The downstream ports in PM L1 stay in this state.

• 当XpressSWITCH 收到来自下游组件（端点或另一台交换机）的L1 退出请求时，如果下游端口之一从ASPM L1 状态退出到recovery状态？，此时上游端口将退出ASPM L1。

然后，上游端口向根联合体发出 L1 退出信号。Root Complex通过向交换机上游端口发送 L1 退出信号来进行响应。当交换机上游端口退出 L1 时，ASPM L1 中的所有下游端口也退出 L1，以最大限度地减少返回 L0 的总体退出延迟。 PM L1 中的下游端口保持此状态。

ASPM：？？？？

• When the XpressSWITCH receives an L1 exit request from an upstream component (Root Complex or another Switch), the XpressSWITCH upstream port exits the ASPM L1 state. All downstream ports in ASPM L1 will also exit L1 as soon as they detect that the upstream port has exited L1. The downstream ports in PM L1 stay in this state.

• 当XpressSWITCH 收到来自上游组件（Root Complex 或另一个交换机）的L1 退出请求时，XpressSWITCH 上游端口退出ASPM L1 状态。 ASPM L1 中的所有下游端口一旦检测到上游端口已退出 L1，也将立即退出 L1。 PM L1 中的下游端口保持此状态。

Note: The XpressSWITCH can enter L1 states when one or more of its ports is in non-active state (no active data link is present) to enable further power optimization

注意：当一个或多个端口处于非活动状态（不存在活动数据链路）时，XpressSWITCH 可以进入 L1 状态，以实现进一步的功耗优化。

**4.8 Power Management with CLKREQ#**

**4.8 使用 CLKREQ# 进行电源管理**

CLKREQ# is an optional side-band pin present in some form factors, which enables power saving. It is used by the Clock Power Management and L1 PM substates with CLKREQ# features. Note that only one of these power saving techniques can be enabled at any one time.

XpressSWITCH uses the following signals for power management with CLKREQ#.

• pl\_clkreq\_oen • pl\_clkreq\_in • tl\_pm\_refclk\_rem • tl\_pm\_l1ss\_status • tl\_pm\_l1ss\_entreq • tl\_pm\_l1ss\_entack See **Section 6.2.9** for a full description of these signals.

CLKREQ# 是某些外形尺寸中存在的可选边带引脚，可实现节能。

它由具有**CLKREQ#特性**的“时钟电源管理“和“L1 PM 子状态”使用。请注意，任一时间只能启用这些（这些：二选一？）省电技术中的一种。

**CLKREQ#特性：**是某些外形尺寸中存在的可选边带引脚，可实现节能。

XpressSWITCH 使用以下信号通过 CLKREQ# 进行电源管理。

• pl\_clkreq\_oen • pl\_clkreq\_in • tl\_pm\_refclk\_rem • tl\_pm\_l1ss\_status • tl\_pm\_l1ss\_entreq • tl\_pm\_l1ss\_entack 有关这些信号的完整说明，请参见第 6.2.9 节。

**4.8.1 Clock Power Management**

**4.8.1 时钟电源管理**

Note: **Clock Power Management is a deprecated feature available only in some form factors such as PCIe mini cards;** it is highly recommended that new designs implement L1 PM sub-states instead.

注意：时钟电源管理是一项已弃用的功能，仅在某些外形规格（例如 PCIe 迷你卡）中可用；强烈建议新设计改为实现 L1 PM 子状态。

CLKREQ# functionality is implemented via the Link Capability and Link Control registers in the Configuration Space.

**When multiple functions are enabled, each function must be CLKREQ# capable.**

When CLKREQ# is used to manage power consumption in the L2 state, the MAC transitions from the P0 to the P2 low power state to stop the Reference Clock, then deasserts CLKREQ#.

CLKREQ# 功能是通过配置空间中的链路功能和链路控制寄存器实现的。

当启用多个功能时，每个功能都必须支持 CLKREQ#。

当 CLKREQ# 用于管理 L2 状态下的功耗时，MAC 将从 P0 转换到 P2 低功耗状态，以停止参考时钟，然后置低 CLKREQ#。

If TL\_PM\_REFCLK\_REM is set to 1 when entering the L1 state, then the MAC transitions from P0 to P2 directly, instead of finishing in P1. When transitioning out of the L1 or L2 states, CLKREQ# is asserted to re-start the Reference Clock.

The following waveform illustrates an L1 entry where the application does not allow clock removal (TL\_PM\_REFCLK\_REM=0), followed by an L1 entry where the application does allow clock removal (TL\_PM\_REFCLK\_REM=1)

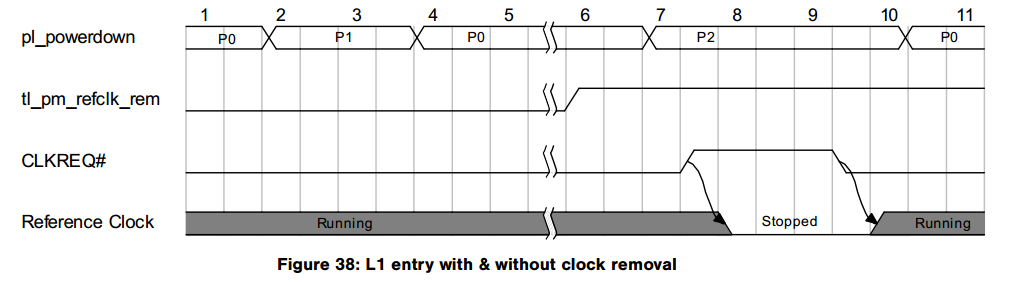
如果进入 L1 状态时， TL\_PM\_REFCLK\_REM 设置为 1，则 MAC 直接从 P0 转换到 P2，而不是在 P1 结束。

当转换出 L1 或 L2 状态时（即：转换完毕后，不在L1或L2状态），**CLKREQ# 被置位以重新启动参考时钟**。

以下波形说明：

应用程序**不允许**时钟移除 (TL\_PM\_REFCLK\_REM=0) 的 L1 entry ，

随后是应用程序**允许**时钟移除 (TL\_PM\_REFCLK\_REM=1) 的 L1 entry。



Note: While specifications define Clock Power Management for x1 mobile form factors only, there is no limitation in the XpressSWITCH Core itself, so CLKREQ# can be implemented for any lane configuration.

注意：虽然文档仅针对 x1 移动设备外形尺寸定义了时钟电源管理，但 XpressSWITCH 内核本身没有限制，因此可以针对任何通道配置实施 CLKREQ#。

When using Clock Power Management, the **PIPE clock (PL\_PCLK)** can be stopped when the PHY is in the P2 state.

The **Transaction Layer clock (TL\_CLK)** must continue to run, however, even if at a very low frequency, so that any traffic on the Transaction Layer Transmit interface will cause the Core to assert CLKREQ# and exit low-power.

使用时钟电源管理时，当 PHY 处于 P2 状态时，可以停止 PIPE 时钟 (PL\_PCLK)。

然而，事务层时钟 (TL\_CLK) 必须继续运行，即使频率非常低。

因此（此时？）事务层发送接口上的任何流量都会导致内核断言 CLKREQ# 并退出低功耗模式。

**PIPE clock (PL\_PCLK)？？**

**Transaction Layer clock (TL\_CLK)？？**

内核断言 CLKREQ#，不应该是关闭时钟，进入低功耗模式吗？

**4.8.2 L1 PM Substates with CLKREQ#**

**4.8.2 L1 PM 子状态与 CLKREQ#**

L1 PM sub-states is an addition to the PCI Express Specification that enables deep power savings in the L1 and ASPM L1 states.

L1 PM 子状态是 PCI Express 规范的补充，可在 L1 和 ASPM L1 状态下实现深度节能。

P.S：说明这是专有特性！！

**4.8.2.1 Enabling L1 PM Sub-States**

**4.8.2.1 使能L1 PM 子状态**

L1 PM sub-states are configured via the L1 PM sub-states capability and the T\_POWEROFF parameter (K\_PEXCONF[263:261], see Section 6.1.3). The configuration of these sub-states also requires that Latency Tolerance Reporting is implemented and properly configured. Values for TL\_REPORT\_LATENCY must always be valid as they are used to check if L1 sub-state entry is possible.

L1 PM 子状态通过L1 PM 子状态功能和T\_POWEROFF 参数（K\_PEXCONF[263:261]，参见第6.1.3 节）进行配置。这些子状态的配置还要求实现并正确配置延迟容忍报告。 TL\_REPORT\_LATENCY 的值必须始终有效，因为它们用于检查是否可以进入 L1 子状态。

In order to verify that the Core is configured properly, you can check TEST\_OUT[93:90] to verify which sub-states are enabled and can be entered from L1

为了验证Core配置是否正确，您可以检查TEST\_OUT[93:90]来验证哪些子状态已启用并且可以从L1进入。

**4.8.2.2 Sub-States Entry/Exit**

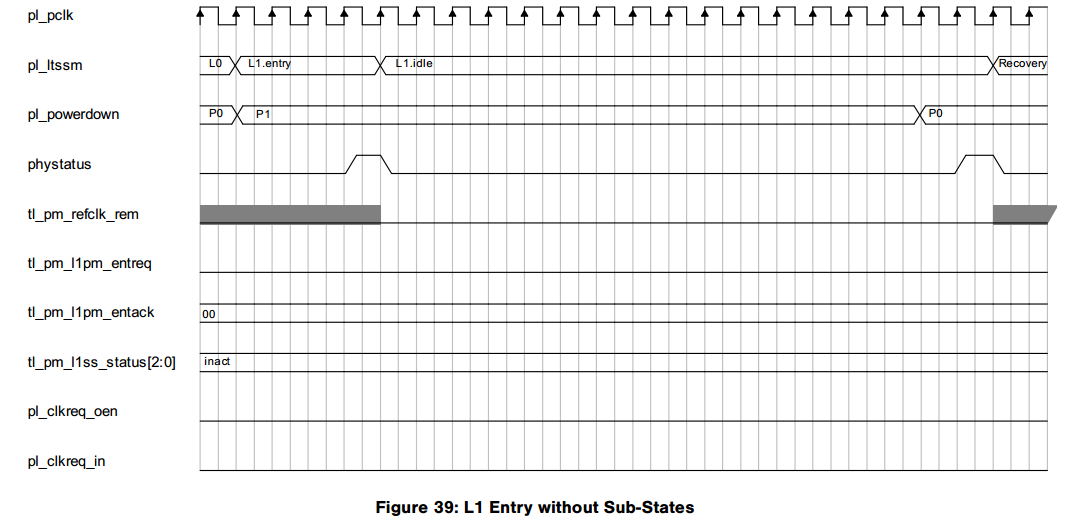
**4.8.2.2 子状态进入/退出**

Whenever the Core enters the L1 state, it checks if all conditions are met to enter a substate.

If no suitable sub-state is enabled or the application does not allow REFCLK removal (TL\_PM\_REFCLK\_REM=0), then the Core enters L1 and does not take any further action. This is illustrated in the waveform below:

每当Core 进入L1 状态时，它都会检查是否满足进入子状态的所有条件。

如果没有启用合适的子状态或应用程序不允许移除 REFCLK (TL\_PM\_REFCLK\_REM=0)，则内核进入 L1 并且不采取任何进一步操作。下面的波形图说明了这一点：



If a suitable sub-state is enabled and the application allows REFCLK removal (TL\_PM\_REFCLK\_REM=1) then the Core:

1. Enters the Entry state, where it requests the PHY to prepare for possible L1 sub-state entry.

2. When all PHY lanes have acknowledged this request (the PHY can turn off PL\_PCLK at this point), the Core moves to L1.0 and deasserts CLKREQ#.

3. If CLKREQ# is sampled deasserted, the Core can then enter the L1.1 or L1.2 sub-states.

如果启用了合适的子状态并且应用程序允许移除 REFCLK (TL\_PM\_REFCLK\_REM=1)，则内核需要：

1. 进入Entry state，请求 PHY 为可能的 L1 sub-state（子状态）进入做好准备。

2. 当所有 PHY 通道均响应此请求时（此时 PHY 可以关闭 PL\_PCLK），内核将移至 L1.0 并置低 CLKREQ#。

3. 如果 CLKREQ# 采样为0，则内核可以进入 L1.1 或 L1.2 sub-state（子状态）。

下图中无体现！！！

To exit L1, the Core: 1. First reverts to L1.0, then enters the Exit state where it requests the PHY to prepare for L1 exit.

2. When all PHY lanes have acknowledged this request, and the PHY has turned PL\_PCLK back on, the Core exits L1.

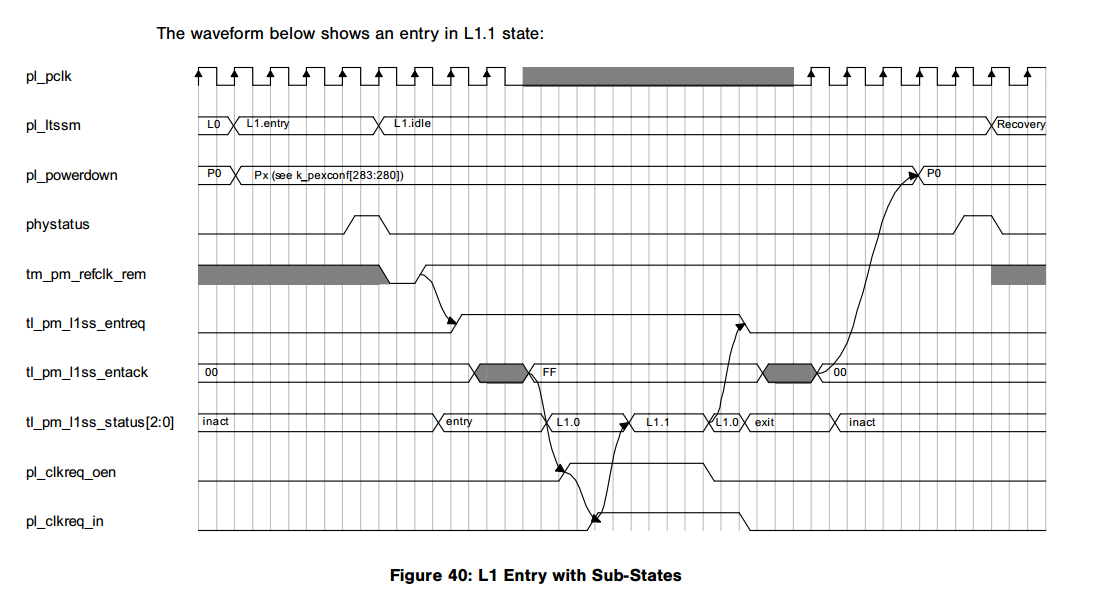
要退出 L1，则内核需要：

1. 首先恢复到 L1.0，然后进入Exit state，请求 PHY 为退出L1做准备。

2. 当所有 PHY 通道均已响应此请求，并且 PHY 已重新打开 PL\_PCLK 时，内核退出 L1。

The waveform below shows an entry in L1.1 state:

下面的波形显示了进入L1.1状态：

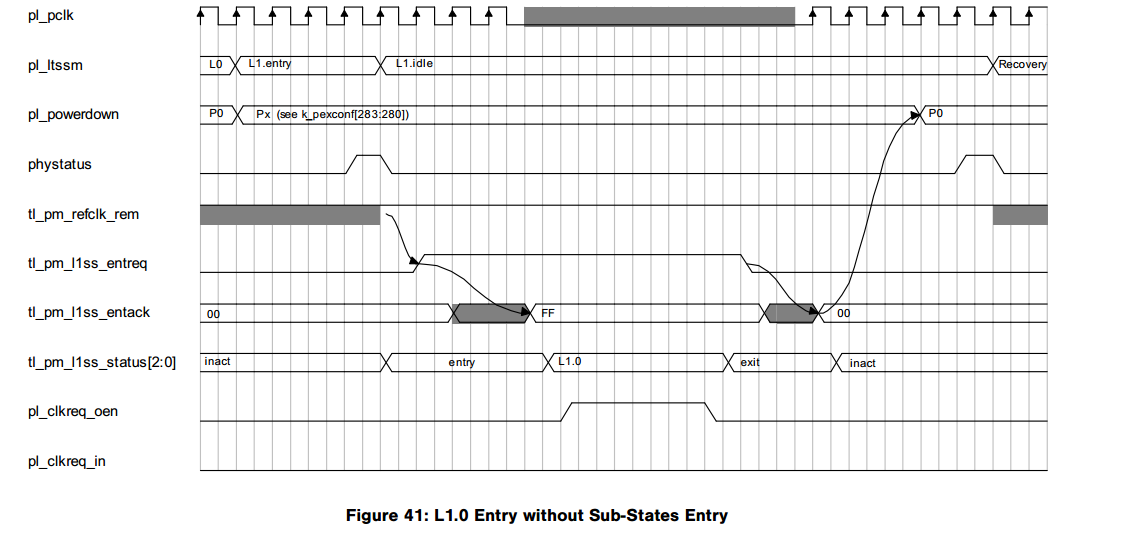


The waveform below shown an entry in L1.0 state, that is not followed by an entry into a sub-state. This can happen if the Core needs to exit L1 before sub-state entry occurs, or if the link partner does not allow sub-state entry:

下面的波形显示了 L1.0 状态的进入，随后没有进入子状态。

如果 Core 需要在进入子状态之前退出 L1，或者link partner不允许进入子状态，则可能会发生这种情况。

P.S：和Figure40的唯一区别是，tl\_pm\_refclk\_rem没有从0-1的过程？这是导致没有进入子状态的原因吗？



Note: When using L1 PM sub-states, the PIPE clock (PL\_PCLK) can be stopped when the Core is in the L1.x sub-states. The Transaction Layer clock (TL\_CLK) must continue to run, however, even if at a very low frequency, so that any traffic on the Transaction Layer Transmit interface will cause the Core to assert CLKREQ# and exit low-power.

注意：使用 L1 PM 子状态时，当内核处于 L1.x 子状态时，PIPE 时钟 (PL\_PCLK) 可以停止。然而，事务层时钟 (TL\_CLK) 必须继续运行，即使频率非常低，因此事务层发送接口上的任何流量都会导致内核断言 CLKREQ# 并退出低功耗。

**4.9 Power Gating**

**4.9 电源门控**

**4.9.1 Enabling Power Gating**

**4.9.1 启用电源门控**

The XpressSWITCH simulation design supports power gating using the IEEE 1801 methodology. To enable this feature, add the “power\_aware” option in the simulation run command line (see Section 7.2).

XpressSWITCH 仿真设计支持使用 IEEE 1801 方法的电源门控。要启用此功能，请在模拟运行命令行中添加“power\_aware”选项（请参见第 7.2 节）。

This option makes a call to the UPF file and adds the required options for the simulation design to run with UPF.

此选项调用 UPF 文件并添加仿真设计与 UPF 一起运行所需的选项。

**4.9.2 Power Domains**

**4.9.2电源域**

The simulation design supports one always-on power domain (**PD\_AON**) and switchable power domains per port (**PD\_SW0**, **PD\_SW1**, etc). As shown in the diagram below, per-port power switches are available in the **PD\_AON** power domain. In this case, when one of the downstream ports goes to the **L1.1**, **L1.2**, or **L2** state, the power management unit can switch the power supply of the corresponding switchable power domain.

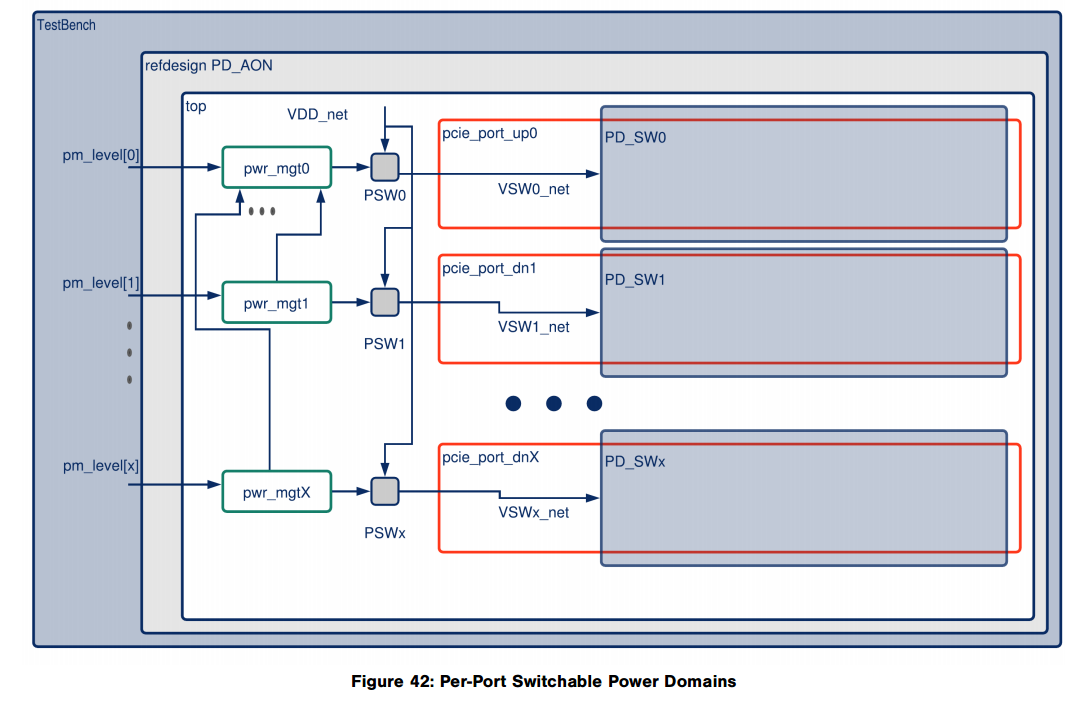
该仿真设计支持每个端口一个常开电源域 (PD\_AON) 和可切换电源域（PD\_SW0、PD\_SW1 等）。如下图所示，PD\_AON 电源域中提供每端口电源开关。在此情况下，当下游端口之一进入L1.1、L1.2或L2状态时，电源管理单元可以切换对应的可切换电源域的电源。

A dedicated power management unit for each port controls the clock gating, isolation, save and restore retention signals and the power switch per switching power domain.

每个端口的专用电源管理单元控制时钟门控、隔离、保存和恢复保留信号以及每个开关电源域的电源开关。

Each power management unit has a **PM\_LEVEL** control. When this input is set, the current power management unit can go to a deep power-down level and switch off the corresponding switchable power domain. If this input is not set, the lowest power level is clock gating for the corresponding port.

每个电源管理单元都有一个 PM\_LEVEL 控制。当该输入被设置时，当前电源管理单元可以进入深度断电级别并关闭相应的可切换电源域。如果未设置此输入，则最低功率级别是相应端口的时钟门控。



**4.9.3 Clock Gating Strategy**

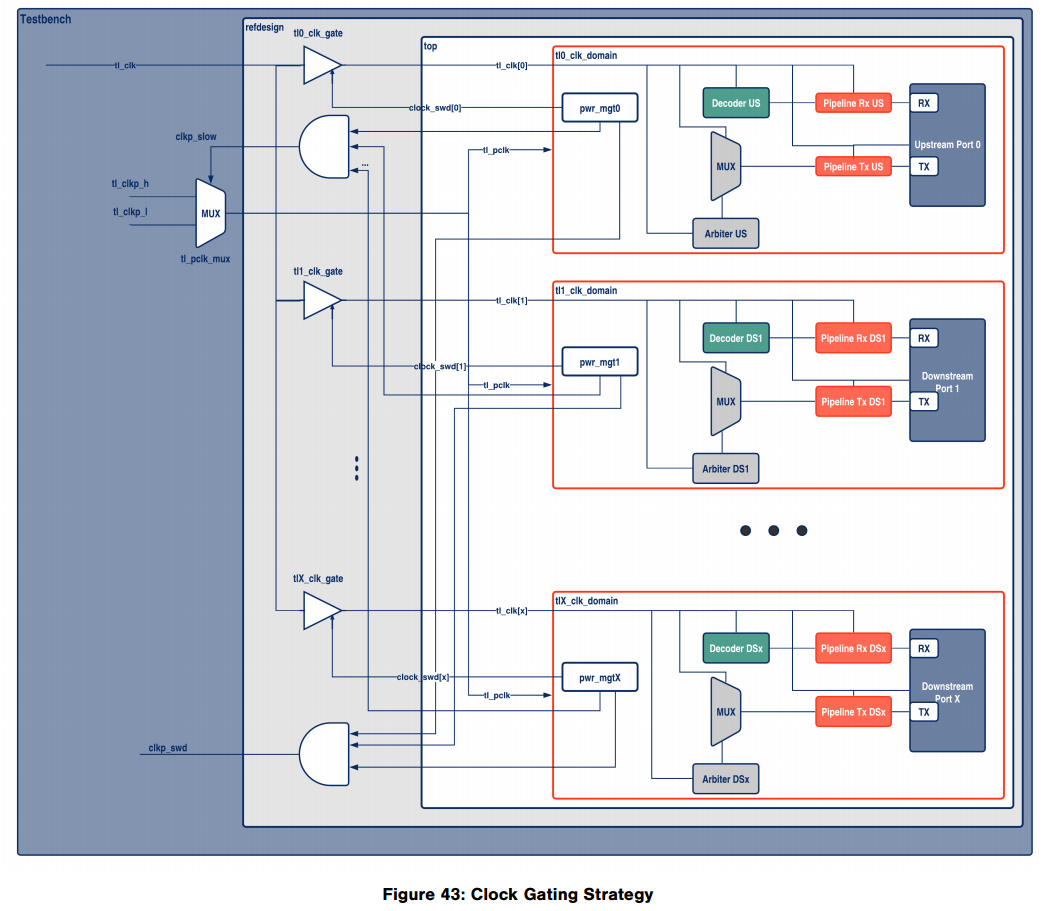
**4.9.3时钟门控策略**

The current clock gating strategy uses clock gaters for each port. The control for each clock gater is provided from the corresponding power management unit. When all downstream ports and the upstream port are clock-gated, the switch can send a signal to lower the frequency of the TL\_CLKP clock for additional power savings.

当前的时钟门控策略对每个端口使用时钟门控。每个时钟选通器的控制由相应的电源管理单元提供。当所有下游端口和上游端口都是可门控时钟，交换机可以发送信号来降低 TL\_CLKP 时钟的频率，以进一步节省功耗。

The following picture shows the clock gating scheme:

下图为时钟门控方案：



A CLKP\_SLOW output controls the TL\_CLKP clock frequency. When all ports are in low power mode, the TL\_CLKP clock frequency can be switched to a lower frequency using this control.

**CLKP\_SLOW** 输出控制 **TL\_CLKP** 时钟频率。当所有端口都处于低功耗模式时，可以使用此控制将 **TL\_CLKP** 时钟频率切换到较低频率。

Note: For backward compatibility, the CLKP\_SWD output clock-gates the **TL\_CLKP** clock when all ports are in **L12 Idle** mode. This output can be used in both clock-gating and power gating modes.

注：为了向后兼容，当所有端口都处于 L12 空闲模式时，CLKP\_SWD 输出时钟对**TL\_CLKP** 时钟进行门控。该输出可用于时钟门控和电源门控模式。

Note: The clock gaters shown in the simulation design above are only models and should be replaced with real clock gates.

注意：上面的仿真设计中显示的时钟门电路只是模型，应替换为真实的时钟门电路。

**4.9.4 Power Management Unit**

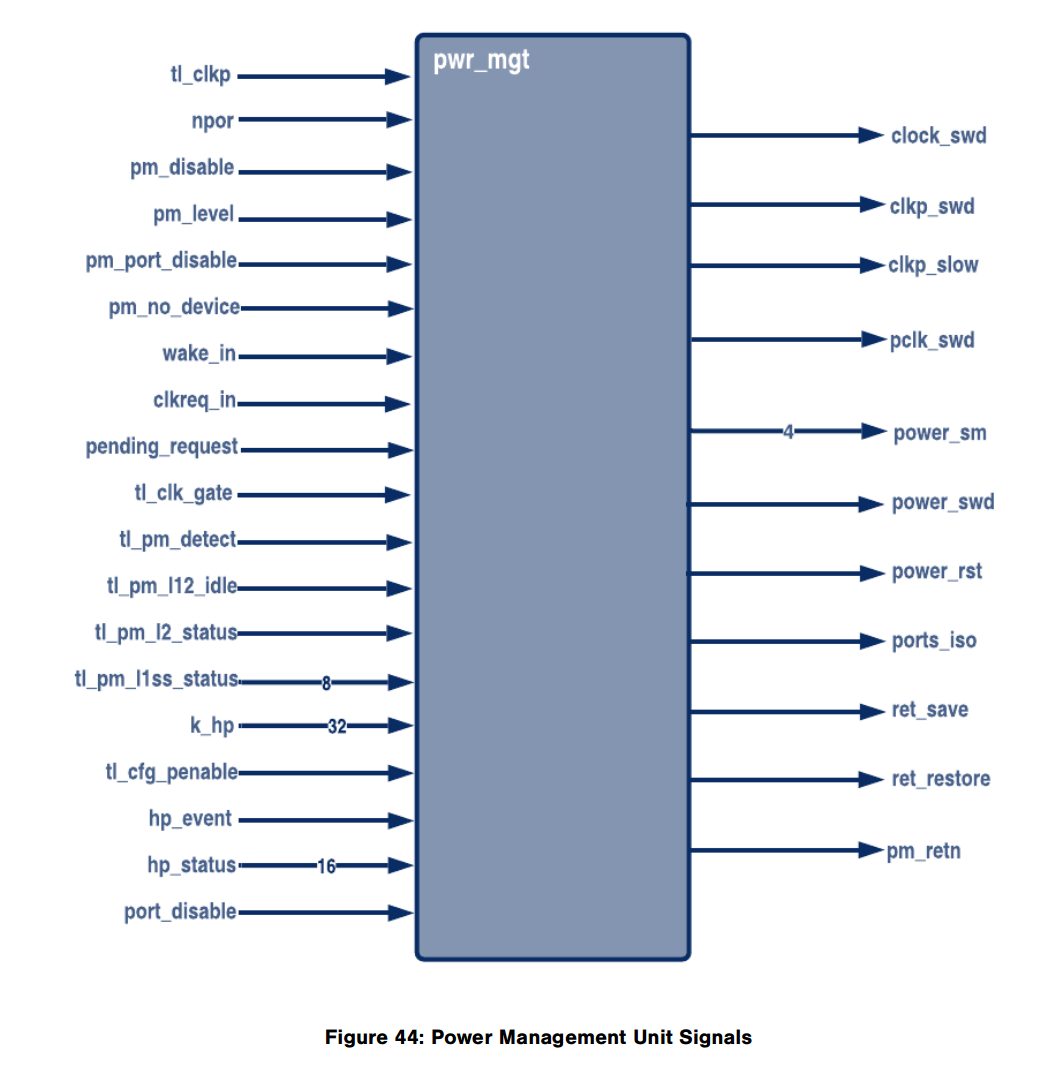
**4.9.4 电源管理单元**

**4.9.4.1 Power Management Unit Signals**

**4.9.4.1 电源管理单元信号**

The following diagram shows the input and output signals of the power management unit.

下图显示了电源管理单元的输入和输出信号。



The following table describes the power management unit signals. The power management unit uses the TL\_CLKP clock.

下表描述了电源管理单元信号。电源管理单元使用TL\_CLKP时钟。

|  |  |  |  |
| --- | --- | --- | --- |
| Name | I/O | Size | Description |
| tl\_clkp | In | 1 | Input clock for the power management unit. This signal should always be active  电源管理单元的输入时钟。该信号应始终有效 |
| npor | In | 1 | Asynchronous power-on reset.  异步上电复位。 |
| pm\_disable | In | 1 | Disable power mode:  Set to 1 to disable all low power modes, even clock gating.、  禁用功耗模式：  设置为 1 可禁用所有低功耗模式，甚至时钟门控。 |
| pm\_level | In | 1 | Power level control:  •1’b0: Clock gating only  •1’b1: Power down for the switchable power domain  Note: If you do not require power gating, you can tie this signal to 0.  功率控制等级：  • 1’b0：仅时钟门控  • 1’b1：可切换电源域断电  注意：如果不需要功率门控，可以将此信号连接至 0。 |
| wake\_in | In | 1 | Wake input event signal  唤醒输入事件信号 |
| pending\_request | In | 1 | Pending transaction request  待处理的交易请求 |
| tl\_clk\_gate | In | 1 | TL\_CLK gating input request  TL\_CLK 门控输入请求 |
| tl\_pm\_l12\_idle | In | 1 | L12\_IDLE power state indication  L12\_IDLE电源状态指示 |
| clkreq\_in | In | 1 | CLKREQ# input  CLKREQ# 输入 |
| tl\_pm\_l2\_status | In | 1 | L2 power state indication  L2电源状态指示 |
| tl\_pm\_l1ss\_status | In | 8 | L1SS state  L1SS状态 |
| tl\_cfg\_penable | In | 1 | APB PENABLE input: used to detect APB transactions in the corresponding port.  APB PENABLE 输入：用于检测相应端口中的 APB 事务。 |
| pm\_port\_disable | Out | 1 | Enable power/clock gating in a disabled downstream port:  When set, power/clock gating will be applied to the corresponding downstream port when it is disabled by software.  This signal should be 0 for upstream ports.  在禁用的下游端口中启用电源/时钟门控：  设置后，当被软件禁用时，电源/时钟门控将应用于相应的下游端口。  对于上游端口，该信号应为 0。 |
| pm\_no\_device | Out | 1 | Enable power/clock gating to a downstream port that is configured to support hot-plug but is not connected to a device.  对配置为支持热插拔但未连接到设备的下游端口启用电源/时钟门控。 |
| tl\_pm\_detect | Out | 1 | Input showing that the core is in Detect state.  输入信号，用于表示Core处于检测状态 |
| k\_hp | Out | 32 | Hot-Plug configuration controls  热插拔配置控制 |
| hp\_event | Out | 1 | Hot-Plug wake event  热插拔唤醒事件 |
| hp\_status | Out | 16 | Hot-Plug status provided by the Hot-Plug Controller  热插拔状态(由热插拔控制器提供) |
| port\_disable | Out | 1 | Port Disable:  Shows if the corresponding port is disabled by software.  端口禁用：  显示相应端口是否被软件禁用。 |
| pm\_retn | Out | 1 | Switchable power domain retention control:  •1=Normal mode  •0=Save mode Used when retention flops with only one control are present in the design.  可切换电源域保留控制：  • 1= 正常模式  • 0= 保存模式  仅当设计中存在一个单独控制的保留触发器（retention flops）时使用。 |
| clock\_swd | Out | 1 | TL\_CLK clock gating control output  TL\_CLK时钟门控输出 |
| clkp\_swd | Out | 1 | TL\_CLKP gating control output  TL\_CLKP时钟门控输出 |
| clkp\_slow | Out | 1 | TL\_CLKP clock frequency control  TL\_CLKP 时钟频率控制 |
| pclk\_swd | Out | 1 | PL\_CLK clock gating control output  PL\_CLK时钟门控输出 |
| power\_sm | Out | 4 | Power management unit FSM state  电源管理单元FSM状态 |
| power\_swd | Out | 1 | Power switch control signal  电源开关控制信号 |
| power\_rst | Out | 1 | Switchable power domain reset control  可切换电源域复位控制 |
| ports\_iso | Out | 1 | Switchable power domain output isolation control  可切换电源域输出隔离控制 |
| ret\_save | Out | 1 | Switchable power domain retention save signal  可切换电源域保留信号 |
| ret\_restore | Out | 1 | Switchable power domain retention restore signal  可切换电源域保留恢复信号 |

**4.9.5 Power Management Unit FSM**

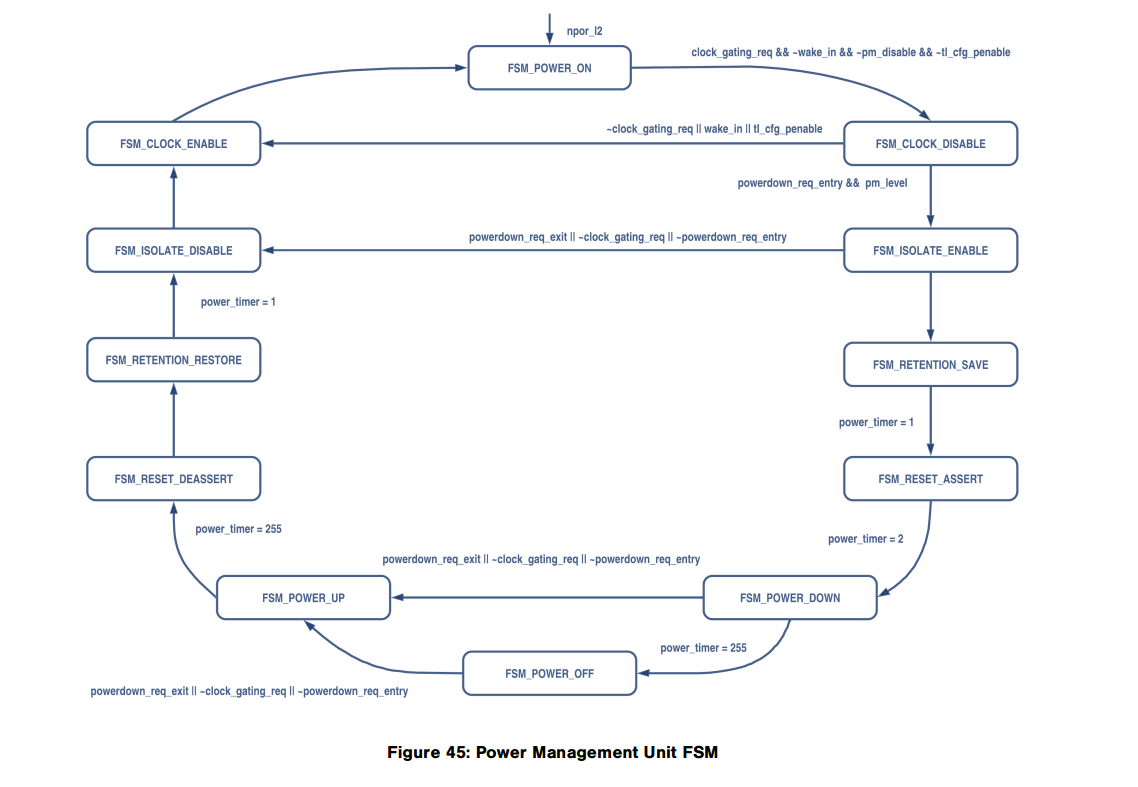
**4.9.5 电源管理单元FSM**

The following diagram shows the FSM (Finite State Machine) of the power management unit and the conditions for switching between the different power states.

下图显示了电源管理单元的FSM（有限状态机）以及不同电源状态之间切换的条件。

The **PM\_DISABLE** input signal to the power management unit enables low-power mode, including clock gating, to be completely disabled.

电源管理单元的 **PM\_DISABLE** 输入信号使低功耗模式（包括时钟门控）能够完全禁用。



The **PM\_LEVEL** signal directly controls the FSM states.

When this control bit is set, the state machine can start the power-down procedure (isolation, save retention, reset, and power down).

When this control bit is 1’b0, the FSM is limited to the clock gating states.

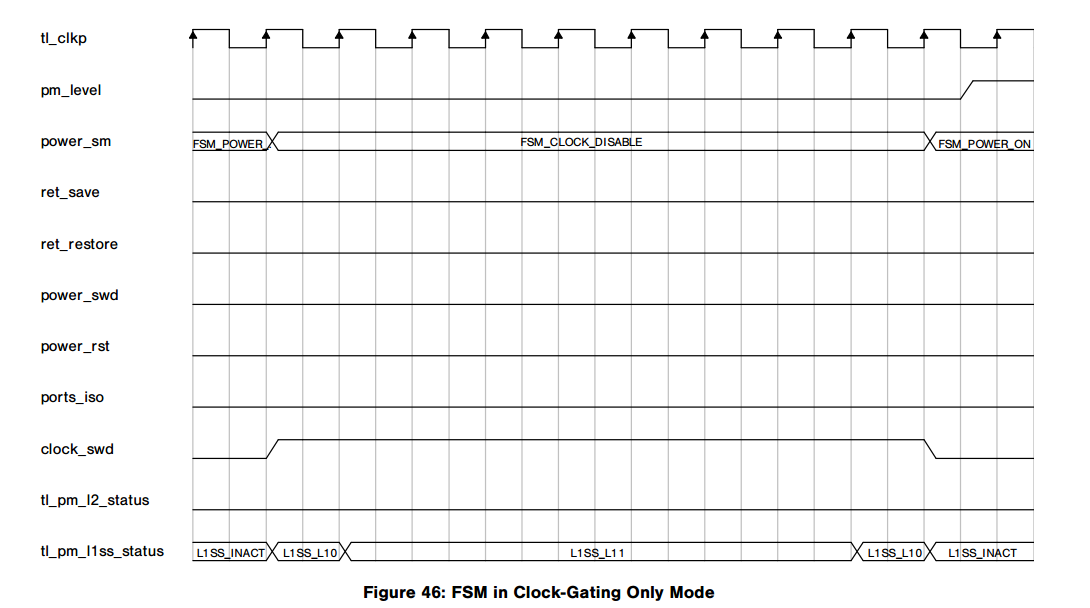
**PM\_LEVEL** 信号直接控制 FSM 状态。

当该控制位为 1’b1 时，状态机可以启动掉电程序（隔离、保存保留、复位和掉电）。

当该控制位为 1’b0 时，FSM 仅限于时钟门控状态。

The following waveform shows the FSM states in clock-gating only mode (PM\_LEVEL = 0) and **L1SS** in **L1.1**.

以下波形显示仅时钟门控模式 (PM\_LEVEL = 0) 和 **L1.1** 中的 **L1SS** 下的 FSM 状态。



The signals shown above are from the power management unit of the upstream port. In this case, since all downstream ports are in clock-gated mode, the upstream port can also go into clock-gated mode and sends a signal to lower the frequency of the TL\_CLKP.

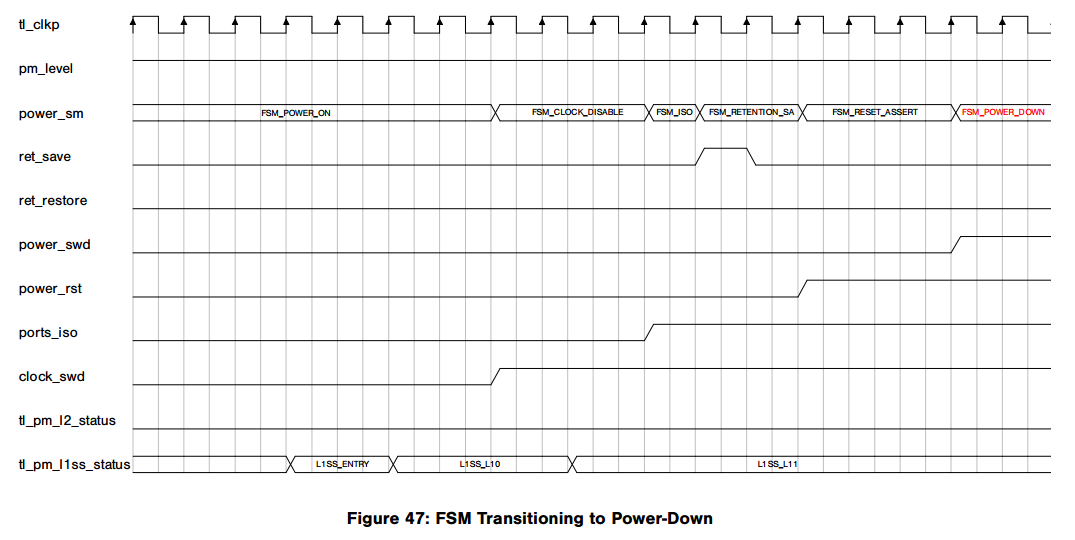
上图所示信号来自上行端口的电源管理单元。在这种情况下，由于所有下游端口都处于时钟门控模式，因此上游端口也可以进入时钟门控模式并发送信号以降低 TL\_CLKP 的频率。

Note: If clock gating is used at all ports and power gating is not required, do not use the provided UPF file. In this case, no power domains will be created.

注意：如果所有端口均使用时钟门控且不需要电源门控，则请勿使用提供的 UPF 文件。在这种情况下，不会创建任何电源域。

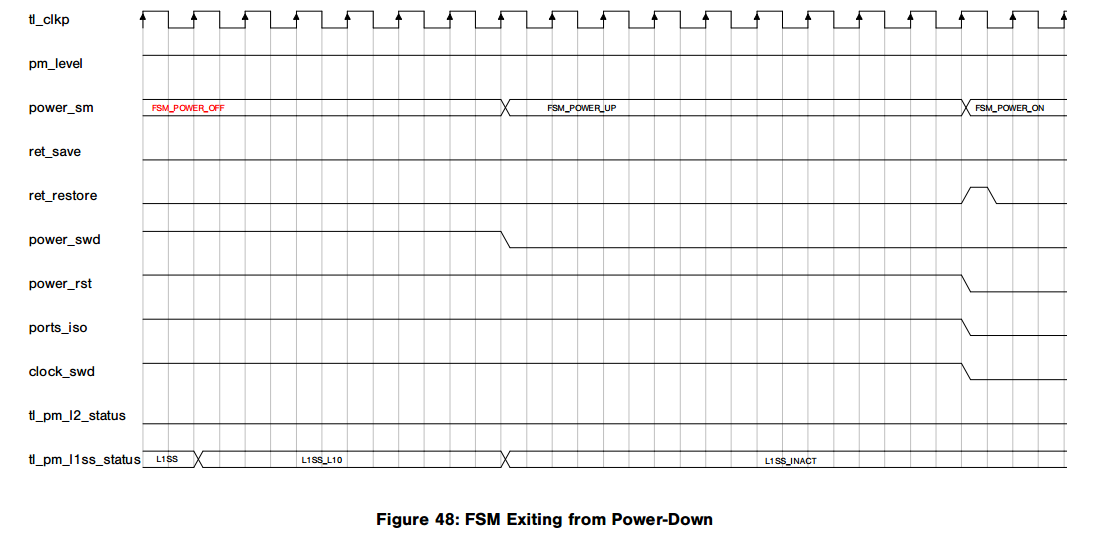
The next timing diagram shows the FSM transitioning from active state to power-down state. In this case, the PM\_LEVEL is 1’b1.

下一个时序图显示 FSM 从活动状态转换到断电状态。在本例中，PM\_LEVEL 为 1’b1。



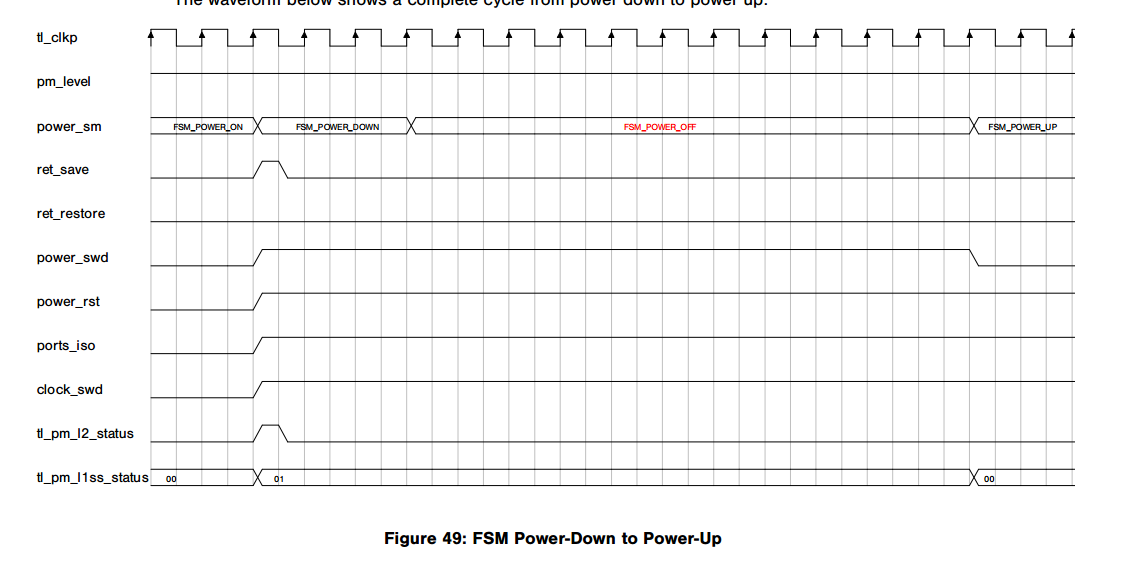
The waveform below shows the exit from power-down:

下面的波形显示了退出掉电的情况：



The waveform below shows a complete cycle from power down to power up:

下面的波形显示了从断电到上电的完整周期：



**4.9.6 Hot-Plug Support**

**4.9.6 热插拔支持**

If a device is configured to support the Hot-Plug, you can configure the XpressSWITCH to clock or power gate this port by setting the PM\_NO\_DEVICE input of the corresponding port (see Table 35).

In this case, when the corresponding downstream port has no device present and the Core LTSSM is in Detect state, the Power Management Unit will start the procedure to clock/power gate this port.

如果设备配置为支持热插拔，您可以通过设置相应端口的 **PM\_NO\_DEVICE** 输入来配置 XpressSWITCH 为该端口提供时钟或电源门控（请参见表 35）。

在这种情况下，当相应的下游端口不存在设备且核心 LTSSM 处于检测状态时，电源管理单元将启动对该端口进行时钟/电源门控的过程。

Note: The XpressSWITCH does not manage the power state of the PHY.

注意：XpressSWITCH 不管理 PHY 的电源状态。

If a device is plugged into the downstream port, a wake event will be triggered to wake-up the upstream port.

如果设备插入下游端口，将触发唤醒事件以唤醒上游端口。

**4.9.7 Port Disable Support**

**4.9.7 端口禁用支持**

When a downstream port is disabled by the software and not used, you can enable clock or power gating on this port using the **PM\_PORT\_DISABLE** input to save power (see Table 35). Clock/power gating can be configured per port.

当下游端口被软件禁用且未使用时，您可以使用 **PM\_PORT\_DISABLE** 输入启用此端口上的时钟或电源门控以节省功耗（请参见表 35）。可以为每个端口配置时钟/电源门控。

As a port can only be enabled/disabled during an XpressSWITCH reset, PCI Express compliance problems should not occur.

由于端口只能在 XpressSWITCH 重置期间启用/禁用，因此不会出现 PCI Express 合规性问题。

**6.2.8 Per-Port Power Management Signals**

**6.2.8 按端口的电源管理信号**

The following table describes legacy and native power management signals. All signals are synchronous to TL\_CLK.

下表列出了传统和本地电源管理信号。所有信号均与 TL\_CLK 同步。

|  |  |  |
| --- | --- | --- |
| Signal | I/O | Description |
| pl\_wake\_oen | out | WAKE# Signal Open-Drain Output Control:  This active-low signal controls the WAKE# pin open-drain output. It is asynchronous when PL\_CLK is not available.  This output is used to drive the optional WAKE# pin if it is present:  • For upstream devices: this pin drives the wake-up mechanism in the L2 state.  • For downstream devices: this pin is used for the OBFF mechanism, if implemented.  When unused this output can be left open  WAKE# 信号开漏输出控制：  该低电平有效信号控制 WAKE# 引脚开漏输出。当 PL\_CLK 不可用时，它是异步的。  该输出用于驱动可选的WAKE# 引脚（如果存在）：  • 对于上游设备：该引脚驱动L2 状态下的唤醒机制。  • 对于下游设备：该引脚用于OBFF 机制（如果已实现）。  不使用时，该输出可以保持开路 |
| pl\_wake\_in | in | WAKE# Signal Input:  This signal reads the state of the WAKE# pin.  This input is used to read the state of optional WAKE# pin if it is present:  • For upstream devices: this pin is used for the OBFF mechanism, if implemented.  • For downstream devices: this pin is used for the wake-up mechanism in the L2 state.  When unused this input must be tied to 1.  WAKE# 信号输入：该信号读取 WAKE# 引脚的状态。  该输入用于读取可选WAKE# 引脚（如果存在）的状态：  • 对于上游设备：该引脚用于OBFF 机制（如果已实现）。  • 对于下游设备：该引脚用于L2 状态下的唤醒机制。  未使用时，该输入必须连接至 1。 |
| tl\_pm\_axupwr | in | Auxiliary Power Detected:  This signal is asserted when auxiliary power is detected. This signal is available as an input when the Wizard option Vaux power detected signal is selected.  检测到辅助电源：  当检测到辅助电源时，该信号被置位。当选择向导选项 Vaux 电源检测到的信号时，该信号可用作输入。 |

**Table 38: Bridge/Switch interface**

**表 38：桥接器/交换机接口**

|  |  |  |
| --- | --- | --- |
| Signal | I/O | Description |
| tl\_brsw\_in[7:0] | in | Bridge/Switch Input:  • Bit 0:  • Switch downstream port: a rising edge of this signal should cause LTSSM to transition to HotReset, and remain in this state as long as this bit is asserted.  Note: This only applies when the LTSSM is in L0 or Recovery state.  • Other:  reserved  • Bit 1:  • Switch upstream port: level sensitive, indicates that the upstream port can enter L1/ASPM L1. This bit must be asserted once all downstream ports are in L1/ASPM L1 and all upstream traffic has been transmitted. It must be de-asserted as soon as one of the downstream ports exits L1/ASPM L1.  • Switch downstream port: level sensitive, indicates that upstream port is in L1/ASPM L1  • Other: reserved  • Bit 2:  • Switch upstream port: a pulse indicates L0s exit on downstream port  • Switch downstream port: a pulse indicates L0s exit on upstream port  • Other: reserved  • Bit 3: Switch upstream port: a pulse indicates that a wake-up event occurred (beacon received or WAKE# asserted) in one of the downstream ports (other: reserved)  • Bit 4: Bridge forward (PCIe-PCI(-X) bridge): level sensitive: indicates that PME# pin is asserted on secondary side (other: reserved)  • Bit 5: Bridge forward (PCIe-PCI(-X) bridge): a pulse asserts “secondary discard timer expired bit” (other: reserved)  • Bit 6: Allow L0s entry:  • Switch upstream port: level sensitive, indicates that none of the switch’s downstream ports are in L0, Recovery, or Configuration states; and that there are no pending TLPs in switching logic.  • Switch downstream port: level sensitive, indicates that switch’s upstream port is not in L0, Recovery, or Configuration states; and that there are no pending TLPs in switching logic.  • Other: reserved  • Bit 7: reserved  桥接/开关输入：  • 位0：  • 开关下游端口：该信号的上升沿应导致LTSSM 转换至HotReset，并且只要该位被置位，就保持在此状态。  注意：这仅适用于 LTSSM 处于 L0 或恢复状态时。  • 其他：保留  • Bit 1：  • 开关上行端口：电平敏感，表示上行端口可以进入L1/ASPM L1。一旦所有下游端口都处于 L1/ASPM L1 并且所有上游流量均已传输，则必须置位该位。一旦下游端口之一退出 L1/ASPM L1，就必须立即取消断言。  • 切换下游端口：电平敏感，表示上游端口处于L1/ASPM L1  • 其他：保留  • Bit 2：  • 切换上游端口：脉冲表示下游端口退出L0  • 切换下游端口：脉冲表示下游端口退出L0上游端口  • 其他：保留  • Bit 3：切换上游端口：脉冲指示下游端口之一发生唤醒事件（接收到信标或 WAKE# 有效）（其他：保留）  • Bit 4：桥接转发（ PCIe-PCI(-X) 桥接器）：电平敏感：表示 PME# 引脚在次级侧有效（其他：保留）  • Bit 5：桥接前向（PCIe-PCI(-X) 桥接器）：脉冲断言“次级”丢弃计时器过期位”（其他：保留）  • Bit 6：允许 L0 条目：  • 交换机上游端口：电平敏感，表示交换机的下游端口均不处于 L0、恢复或配置状态。并且切换逻辑中没有待处理的 TLP。  • 交换机下行端口：电平敏感，表示交换机上行端口不处于L0、Recovery 或Configuration 状态。并且切换逻辑中没有待处理的 TLP。  • 其他：保留  • Bit 7：保留 |
| tl\_brsw\_out[7:0] | out | Bridge/Switch Output:  • Bit 0: Switch upstream and bridge forward (PCIe-PCI(-X) bridge): this bit is asserted when LTSSM is in the HotReset state; it is pulsed when the Secondary Bus Reset register is asserted. (other: reserved)  • Bit 1: Switch upstream & switch downstream: level sensitive, indicates that port is in L1 (other: reserved)  • Bit 2: Switch upstream & downstream: a pulse indicates L0s exit (other: reserved)  • Bit 3: Switch downstream: a pulse indicates that a wake-up event (beacon received) occurred (other: reserved)  • Bit 4:5: reserved  • Bit 6: Port idle indicator:  • Switch upstream and switch downstream: level sensitive; reports that LTSSM is not in L0, Recovery, or Configuration states.  • Other: reserved  • Bits 7: reserved  桥接/开关输出：  - Bit 0：上游开关和桥接前向（PCIe-PCI(-X) 桥接）：当 LTSSM 处于热复位状态时，该位断言；当辅助总线复位寄存器断言时，该位脉冲。(其他：保留）  - Bit 1：上游开关和下游开关：电平敏感，指示端口处于 L1（其他：保留）  - Bit 2：上游开关和下游开关：脉冲指示 L0s 退出（其他：保留）  - Bit 3：下游开关：脉冲指示发生唤醒事件（收到信标）（其他：保留）  - Bit 4:5：保留  - Bit 6：端口空闲指示器：  - 交换机上游和交换机下游：电平敏感；报告 LTSSM 未处于 L0、恢复或配置状态。  - 其他：保留  - Bit 7：保留 |

**6.2.9 Per-Port CLKREQ# Management Signals**

**6.2.9每个端口的CLKCLK #管理信号**

The following table describes the interface signals used with CLKREQ#:

下表描述了与CLKCLK #一起使用的接口信号：

|  |  |  |
| --- | --- | --- |
| Signal | I/O | Description |
| pl\_clkreq\_oen | out | CLKREQ# enable:  Open-drain control for CLKREQ# output:  • When 0: CLKREQ# drives 0  • When 1: CLKREQ# is in high-impedance  This output is used when either Clock Power Management or L1 PM Substates are implemented  CLK # enable：  CLKCLK #输出的开漏控制：  ·0时：CLKCLK #驱动0  ·1时：CLKCLK #处于高阻抗状态  此输出在实现时钟电源管理或L1 PM子状态时使用 |
| pl\_clkreq\_in | in | CLKREQ# input: this signal must be connected to the CLKREQ# line.  It is used when L1 PM substates are implemented.  CLK #输入：此信号必须连接到CLK #线。  当实现L1 PM子状态时使用。 |
| tl\_pm\_refclk\_rem | in | Allow Slot REFCLK Removal: this signal is used by the application to indicate when the PCI Express reference clock can be safely removed (when applicable).  • 0: the application does not allow the reference clock to be removed.  • 1: the application allows the reference clock to be removed.  This signal is not used and must be tied to 0 when Clock Power Management and L1 PM substates with CLKREQ# are not implemented.  允许删除插槽REFCLK：应用程序使用此信号来指示何时可以安全地移除PCI Express参考时钟（在适用时）。  · 0：应用程序不允许删除参考时钟。  · 1：应用程序允许移除参考时钟。  当时钟电源管理和L1 PM子状态与CLKCLK #未实现时，不使用此信号，必须将其连接到0。 |
| tl\_pm\_l1ss\_status[7:0] | out | L1 Sub-States Status:  • bits 2:0: current state:  • 000: Inactive: default, means that either LTSSM is not in the L1 state or the Core is not enabled to enter a L1 sub-state  • 001: L1.1  • 010: L1.2 entry  • 011: L1.2 idle  • 100: L1.2 exit  • 101: L1.0  • 110: Entry: the Core has left Inactive state and is preparing to enter L1.0  • 111: Exit: the Core has left L1.0 and is preparing to revert to Inactive state  • bits 7:3: reserved  L1子状态状态：  ·bits 2:0：当前状态：  · 000：非活动：默认值，表示LTSSM未处于L1状态或内核未被启用以进入L1子状态  · 001：L1.1  · 010：L1.2进入  · 011：L1.2空闲  · 100：L1.2退出  · 101：L1.0  · 110：进入：内核已离开非活动状态并准备进入L1.0  · 111：退出：核心已离开L1.0并准备恢复到非活动状态  ·bits 7:3：保留 |
| tl\_pm\_l1ss\_entreq | out | L1 Sub-States Entry/Exit Request: the Core asserts this signal to indicate that the PHY should prepare for possible L1 sub-state entry, and de-asserts it to indicate that the PHY should prepare for L1 exit.  If L1 sub-states are not supported then this signal can be left unconnected.  L1子状态进入/退出请求：  核心断言该信号以指示PHY应当为可能的L1子状态进入做准备，并且解除断言该信号以指示PHY应当为L1退出做准备。  如果不支持L1子状态，则该信号可以保持未连接。 |
| tl\_pm\_l1ss\_entack  [G\_NUM\_LANES] | in | L1 Sub-States Entry Acknowledgment: PHY reports with this per-lane signal when L1 substates entry/exit preparation is complete:  • each bit of this signal must be asserted following a TL\_PM\_L1SS\_ENTREQ assertion, when the corresponding lane is prepared for L1 sub-state entry.  • each bit of this signal must be de-asserted following a TL\_PM\_L1SS\_ENTREQ de-assertion, when the corresponding lane is ready for L1 exit.  If L1 sub-states are not supported then this signal can be tied to 0; if L1 sub-states are supported but the PHY does not need to perform any entry/exit preparation then this signal must be tied to TL\_PM\_L1SS\_ENTREQ.  L1子状态进入确认：  当L1子状态进入/退出准备完成时，PHY利用该每通道信号进行报告：  ·当相应通道准备用于L1子状态进入时，该信号的每个比特必须在TL\_PM\_L1SS\_ENTREQ断言之后被断言。  ·当相应的通道准备好L1退出时，该信号的每个位必须在TL\_PM\_L1SS\_ENTREQ解除断言之后解除断言。  如果不支持L1子状态，则该信号可以被绑定到0;如果支持L1子状态但PHY不需要执行任何进入/退出准备，则该信号必须被绑定到TL\_PM\_L1SS\_ENTREQ。 |